WE CLAIM:

1. A computer system comprising a plurality of processor clusters, each cluster including a plurality of nodes, the nodes including processors and an interconnection controller interconnected by point-to-point intra-cluster links, each of the processors and the interconnection controller communicating within a cluster via an intra-cluster transaction protocol, inter-cluster links being formed between interconnection controllers of different clusters, each of the processors and the interconnection controller in a cluster having a test interface for communicating with service processor, at least one of the nodes in a cluster is a command-injecting node configured to receive a command via a test interface and to inject the command into a queue of commands according to the intra-cluster transaction protocol.

2. The computer system of claim 1, wherein the test interface is compliant with the Joint Test Action Group standard.

3. The computer system of claim 1, wherein the injected command is selected from the group consisting of (a) a command for reading a configuration of a node within a local cluster that includes the service processor that made the injected transaction; (b) a command for writing a configuration of a node within a local cluster that includes the service processor that made the injected transaction; (c) a command for reading a configuration of a node within a remote cluster that does not include the service processor that made the injected transaction; and (d) a command for writing a configuration of a node within a remote cluster that does not include the service processor that made the injected transaction.

4. The computer system of claim 1, wherein the injected command comprises a new transaction.

5. The computer system of claim 1, wherein the injected command comprises a part of a transaction that was in progress before the command was injected.

6. The computer system of claim 1, wherein the interconnection controllers communicate between clusters via an inter-cluster transaction protocol.

7. The computer system of claim 1, wherein the test interface further comprises a mailbox register for receiving the command.

8. The computer system of claim 1, wherein a command is received from the test interface in a first clock domain and at least part of the command-injecting node operates in a second clock domain, and wherein the command-injecting node is further configured for:

receiving injected transactions in the first clock domain; and

synchronizing the injected transactions to the second clock domain.

9. The computer system of claim 1, wherein the command-injecting node is an interconnection controller.

10. The computer system of claim 1, wherein the command-injecting node is any device capable of driving the JTAG port.

11. The computer system of claim 4, wherein the new transaction is within a local cluster that includes the command-injecting node.

12. The computer system of claim 4, wherein the new transaction is within a remote cluster that includes the command-injecting node.

13. The computer system of claim 7, wherein the mailbox register is configured to be connected with a test data in interface and a test data out interface.

14. An interconnection controller for use in a computer system comprising a plurality of processor clusters, each cluster including a plurality of nodes, the nodes including processors and an instance of the interconnection controller interconnected by point-to-point intra-cluster links, each of the processors and the interconnection controller within a cluster communicating via an intra-cluster transaction protocol, the interconnection controller configured to receive commands via a test interface and to inject the commands into a queue of pending commands according to the intra-cluster transaction protocol.

15. The interconnection controller of claim 14, wherein a service processor in a cluster that includes the interconnection controller operates in a first clock domain, wherein the interconnection controller operates in a second clock domain, and wherein the interconnection controller is further configured for:

receiving injected transactions from the service processor in the first clock domain; and

synchronizing the injected transactions to the second clock domain.

16. The interconnection controller of claim 14, further comprising a mailbox register for receiving the injected transaction from the service processor.

17. An integrated circuit comprising the interconnection controller of claim 14.

18. At least one computer-readable medium having data structures stored therein representative of the interconnection controller of claim 14.

19. A set of semiconductor processing masks representative of at least a portion of the interconnection controller of claim 14.

20. The integrated circuit of claim 17, wherein the integrated circuit comprises an application-specific integrated circuit.

21. The at least one computer-readable medium of claim 18, wherein the data structures comprise a simulatable representation of the interconnection controller.

22. The at least one computer-readable medium of claim 18, wherein the data structures comprise a code description of the interconnection controller.

23. The at least one computer-readable medium of claim 21, wherein the simulatable representation comprises a netlist.

24. The at least one computer-readable medium of claim 22, wherein the code description corresponds to a hardware description language.

25. The interconnection controller of claim 14, wherein the queue of pending commands is controlled by a protocol engine, the interconnection controller further configured to process access commands for accessing configuration registers of the interconnection controller without forwarding the access commands to the protocol engine.

26. The interconnection controller of claim 25, further comprising a configuration access unit for processing access commands.